IN THE CLAIMS

Please cancel claims 1-22 without prejudice.

Please amend claims 23-24 and 27-28 as follows below.

Please add new claims 29-37 that follow below.

The following is a listing of claims that will replace all prior versions, and listings, of claims in the application:

Listing of Marked Up Claims:

1- 22. (Cancelled).

23. (Currently Amended) A bipolar transistor, comprising:

a substrate;

a base region having an intrinsic base region and an extrinsic base region;

wherein the extrinsic base region is raised relative to the intrinsic base region;

wherein the extrinsic base region has a thickness *x* and the intrinsic base region has a thickness *y*, and wherein *x* [[>]] is greater than *y*.

24. (Currently Amended) The bipolar transistor of claim 23, further comprising an emitter structure, the emitter structure comprising:

a polysilicon emitter having a first portion with a width *a*, a second portion with a width *b*, and a third portion with a width *c*;

wherein *c* [[>]] is greater than *b* [[>]] which is greater than *a*; and

wherein the first portion defines an emitter base junction, and wherein the third portion defines an emitter contact region.

25. (Original) The bipolar transistor of claim 24, wherein

the emitter region further comprises a nitride spacer directly adjacent to the polysilicon emitter.

26. (Original) The bipolar transistor of claim 23, wherein

the extrinsic base region comprises:

a first epitaxial layer; and

a second epitaxial layer on the first epitaxial layer.

27. (Currently Amended) The bipolar transistor of claim 26, [[where]] wherein

the first epitaxial layer is a SiGe epitaxial layer and

the second epitaxial layer is a heavily p-type doped Si or SiGe epitaxial layer.

28. (Currently Amended) The bipolar transistor of claim 23, wherein

the bipolar transistor is [[being]] an npn transistor.

29. (New) A bipolar transistor, comprising:

a substrate having a collector region, the collector region being a collector terminal;

a first epitaxial silicon layer on a surface of the substrate;

an emitter stack on the first epitaxial silicon layer, the emitter stack being an emitter terminal;

a second epitaxial silicon layer on portions of the first epitaxial silicon layer located outside the emitter stack;

wherein a region of the first epitaxial silicon layer located under the emitter stack is an intrinsic base region and a region of the second epitaxial silicon layer on portions of the first epitaxial silicon layer located outside the emitter stack being a raised extrinsic base region;

wherein the raised extrinsic base region has a thickness greater than a thickness of the intrinsic base region; and

wherein the intrinsic base region and the raised extrinsic base region provide a base terminal of the bipolar transistor with lower resistivity.

30. (New) The bipolar transistor of claim 29, wherein

the first epitaxial layer is a p-type Si, SiGe or SiGe:C epitaxial layer and

the second epitaxial layer is a selectively deposited heavily p-type doped Si epitaxial layer or a selectively deposited heavily p-type doped SiGe epitaxial layer.

31. (New) The bipolar transistor of claim 29, wherein the emitter stack includes

a first oxide layer on the first epitaxial silicon layer;

a first nitride layer on the first oxide layer;

a second oxide layer on the first nitride layer;

ions implanted through an emitter window in the second oxide layer and the first nitride layer to form a polysilicon emitter.

32. (New) The bipolar transistor of claim 29, wherein the bipolar transistor is a Si, SiGe or SiGe:C npn bipolar transistor.

33. (New) A bipolar transistor having a base, a collector, and an emitter, the bipolar transistor comprising:

a substrate with a collector region;

a base region coupled to the substrate, the base region having an intrinsic base region and an extrinsic base region;

a polysilicon emitter structure coupled to the intrinsic base region; and

wherein the extrinsic base region has a thickness X and the intrinsic base region has a thickness *y*, and wherein *X* is greater than *Y*.

34. (New) The bipolar transistor of claim 33, wherein the extrinsic base region is raised relative to the intrinsic base region.

35. (New) The bipolar transistor of claim 33, wherein the polysilicon emitter structure has a first portion providing an emitter base junction, a second portion providing conduction, and a third portion providing an emitter contact region.

36. (New) The bipolar transistor of claim 35, wherein the first portion of the polysilicon emitter structure has a width A,

the second portion of the polysilicon emitter structure has a width B differing from A,

the third portion of the polysilicon emitter structure has a width C differing from A and C.

37. (New) The bipolar transistor of claim 36, wherein the width C is greater than the width B which is greater than the width A.